CLAIMS

What is claimed is:

1. An apparatus comprising:

a cache to provide access to contents of a memory bank;

more than two global buses to provide parallel access to said cache and the memory bank; and

a cache controller to maintain a content of the memory bank in said cache via parallel access of said cache and the memory bank to respond to a request for an access of the memory bank substantially independent of a latency to refresh the memory bank.

2. The apparatus of claim 1, further comprising:

a tag buffer coupled to said cache to associate a cache line with a line of the memory bank; and

a row decoder coupled to the tag buffer to decode a tag stored in the tag buffer.

3. The apparatus of claim 1, further comprising a dirty bit buffer coupled to the cache to indicate a relationship between a line of the cache and a line of the memory bank, wherein the cache controller comprises circuitry to turn on write access to the cache via a first global bus of the more than two global buses during a write-back phase of a cycle in response to turning off read access to the cache via a second global bus of the more than two global buses after a read phase of the cycle.

4. The apparatus of claim 1, wherein the memory bank comprises dynamic random access memory.

5. The apparatus of claim 1, wherein said cache comprises at least part of a second memory bank.

6. The apparatus of claim 1, wherein said more than two global buses comprises two pair of global buses coupled to the memory bank and said cache.

7. The apparatus of claim 1, wherein said cache controller comprises circuitry to read from the memory bank and from said cache substantially simultaneously.

8. The apparatus of claim 1, wherein said cache controller comprises circuitry to write to the memory bank and to write to said cache substantially simultaneously.

9. A method, comprising:

receiving a request for an access for contents of a memory bank;

maintaining a content of the memory bank in a cache;

accessing the contents of the memory bank and the cache substantially in parallel in response to said maintaining and to respond to the request substantially independent of a latency to refresh the memory bank.

10. The method of claim 9, wherein said receiving comprises receiving a request for an access for the memory bank when a refresh is pending.

11. The method of claim 9, wherein said maintaining comprises:

direct mapping a line of the memory bank into the cache; and

storing a tag associated with the line of the memory bank.

12. The method of claim 9, wherein said maintaining comprises determining a refresh conflicts with the access.

13. The method of claim 9, wherein said accessing comprises reading from the memory bank substantially simultaneously with reading from the cache.

14. The method of claim 9, wherein said accessing comprises writing to the memory bank substantially simultaneously with writing to the cache.

15. The method of claim 9, wherein said accessing comprises:

turning off read access to the cache for a first global bus during a cycle; and

turning on write access to the cache for a second global bus during the cycle after turning off read access.

16. A system, comprising:

a core; and

a first cache coupled to the core, said first cache comprising

a second cache to provide access to contents of a memory bank;

more than two global buses to provide parallel access to the second cache and the memory bank;

a cache controller to maintain a content of the memory bank in the second cache via parallel access of the second cache and the memory bank to respond to a request for an access of the memory bank substantially independent of a latency to refresh the memory bank.

17. The system of claim 16, wherein the more than two global buses comprises two pair of global buses coupled to the memory bank and the second cache.

18. The system of claim 16, wherein the cache controller comprises:

circuitry to read from the memory bank and from the second cache substantially simultaneously; and

circuitry to write to the memory bank and to write to the second cache substantially simultaneously.

19. A system comprising:

a processor; and

a memory device coupled to said processor, said memory device comprising

a cache to provide access to contents of a memory bank;

more than two global buses to provide parallel access to the cache and the memory bank;

a cache controller to maintain a content of the memory bank in the cache via parallel access of the cache and the memory bank to respond to a request for an access of the memory bank substantially independent of a latency to refresh the memory bank.

20. The system of claim 19, wherein the cache controller comprises:

circuitry to read from the memory bank and from the cache substantially simultaneously; and

circuitry to write to the memory bank and to write to the cache substantially simultaneously.

21. A machine-readable medium containing instructions, which when executed by a machine, cause said machine to perform operations, comprising:

receiving a request for an access for contents of a memory bank;

maintaining a content of the memory bank in a cache;

accessing the contents of the memory bank and the cache substantially in parallel in response to said maintaining and to respond to the request substantially independent of a latency to refresh the memory bank.

22. The machine-readable medium of claim 21, wherein maintaining comprises direct mapping a line of the memory bank into the cache.

23. The machine-readable medium of claim 22, wherein said accessing comprises:

reading from the memory bank substantially simultaneously with reading from the cache; and

writing to the memory bank substantially simultaneously with writing to the cache.